Active-Matrix Microelectrode Arrays Integrated With Vertically Aligned Carbon Nanofibers

Jungwon Park, Seyeoul Kwon, Seung Ik Jun, Timothy E. Mcknight, Anatoli V. Melechko, Michael L. Simpson, Manjeet Dhindsa, Jason Heikenfeld, and Philip D. Rack

***Abstract*—In this letter, we have successfully integrated vertically aligned carbon nanofibers (VACNFs) onto active matrix thin-film transistor (TFT) and demonstrate a new microelectrode array (MEA) platform. The materials and processes of the bottom gate inverted staggered TFT structure were designed to be compatible with the requisite high-temperature ($\sim$700 °C) and direct current plasma-enhanced chemical vapor deposition VACNF growth process. The critical device integration issues are elaborated, and initial device characteristics are reported. This device platform provides great potential as an advanced MEA for direct cell sensing, probing, and recording with a high electrode density and active addressability.**

***Index Terms*—Active matrix addressing, microelectrode array (MEA), thin-film transistor (TFT), vertically aligned carbon nanofiber (VACNF).**

I. Introduction

MICROELECTRODE arrays (MEA) have been studied to investigate electrogenic cells and tissues by intra/extracellular stimulating and recording. A MEA is an arrangement of typically several tens of electrodes with 100−500-μm pitch, allowing the probing of several sites of an individual cell [1]–[3]. Currently, these devices are fabricated by conventional semiconductor fabrication processes with a low number of electrodes, because each element in the array requires its own contact pad. Therefore, an addressing scheme that enhances the electrode density and number of MEA could increase the amount of information that can be obtained. In addition, cells may not adhere well on the electrodes; consequently, the signal-to-noise ratio is not optimal, and often, the signal is not detected properly.

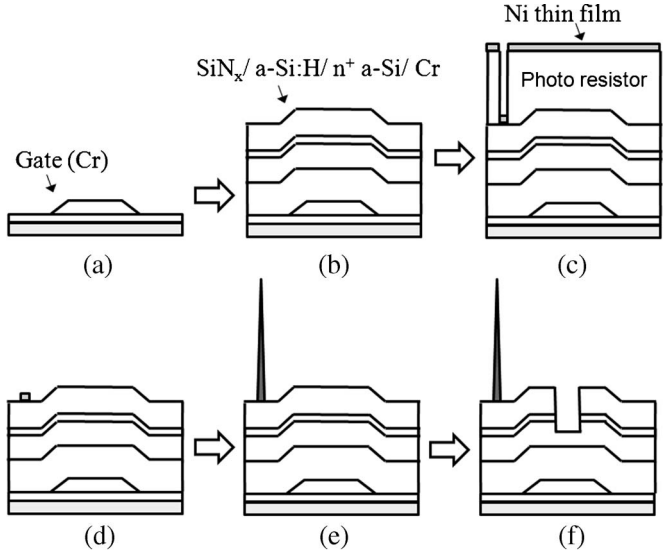


Fig. 1. Schematic illustrating the processing sequence for the TFT-VACNF integration. (a) Cr film deposition and patterned for gate electrode, (b) a-SiN_x, a-Si:H, and n^+ a-Si deposition *in situ* using PECVD following Cr film for S/D electrode deposited, (c) nickel dot patterns are formed on S/D electrodes using conventional photolithography work and Ni deposition by evaporation, and (d) the lift off process. (e) Illustration of the VACNF growth on the nickel catalyst on the uniform chromium layer which is (f) subsequently patterned followed by the active layer back-channel etch process.

To extend the applicability of extracellular and planar MEAs, vertically aligned carbon nanofibers (VACNFs) [4] have been integrated with microstructures for applications such as cell membrane mimics [5], gene delivery arrays [6], neuroelectrochemical interfacing arrays [7], superhydrophobic switches [8], and intracellular probes [9]. In order to increase the number of elements of an MEA and enable both stimulation and recording on the same platform, an actively addressed thin-film transistor (TFT) array was developed. VACNFs were integrated onto the TFT array as they enhance the electrical sensitivity to the cell relative to standard planar arrays; furthermore, the vertical electrodes provide the potential for intracellular sensing within individual cells. To extend the applicability of utilizing these vertical electrodes, here, we describe the integration of VACNFs onto the TFT array.

II. Device Fabrication

For our intracellular probe applications, a bottom gate inverted staggered structure was adopted so the VACNFs could be

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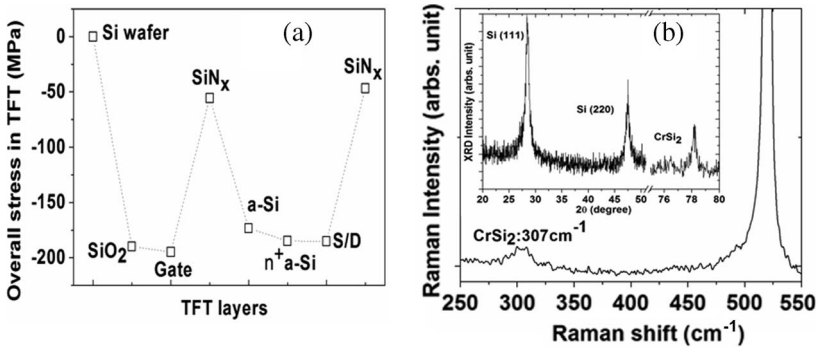


Fig. 2. (a) Cumulative stress measured as a function of each thin-film layer of the TFT device after optimization. (b) Raman and X-ray diffraction spectra of silicon film after VACNF growth (700-°C temperature in dc-PECVD) and wet etching the requisite Cr layer.

integrated onto the drain electrode. Fig. 1 shows the schematic process flow for TFT and VACNF integration. Briefly, plasma-enhanced chemical vapor deposition (PECVD) was used to deposit silicon dioxide (500 nm) on Si wafer; chromium (Cr: 100 nm) was deposited with the radio frequency magnetron sputtering and patterned with a Cr wet etchant. Silicon nitride (SiN_x: 300 nm), hydrogenated amorphous silicon (a-Si:H: 200 nm), and doped amorphous silicon (n^+ a-Si:50 nm) layers were all deposited by PECVD without breaking vacuum. To integrate the VACNFs with the TFT, the standard TFT process flow is slightly varied to accommodate the catalytic synthesis of VACNFs in a direct current (dc)-PECVD process. To facilitate adequate grounding during dc-PECVD process, the VANCFs are grown on the blanket Cr source–drain (S/D) layer (200 nm). VACNF growth requires a catalyst film; thus, $\sim$50-nm-thick and $\sim$1-μm diameter nickel "dots" are patterned onto the drain electrode area. After the nickel is evaporated and patterned via a lift-off process, the VACNFs are grown via a dc-PECVD process using a C_2H_2/NH_3 (85/200 sccm) mixture, 660 W (1 A, constant), 15-torr pressure, 700-°C temperature, and 19 min with a target of $\sim$20-μm-tall fibers. Next, S/D was patterned similar to the gate electrode, and the back channel (n^+ a-Si/a-Si) was etched using a reactive ion etch (RIE) with SF_6/Ar plasma chemistry. After deposition of the passivation SiN_x (300 nm), the electrode contact holes were etched using RIE with SF_6/Ar plasma. One advantage of using Cr electrodes is the fact that the S/D electrodes do not etch during the requisite time for the gate via to etch through active and gate insulator layers.

III. Results and Discussions

Initial VACNF growth attempts resulted in damage to top metallization and arcing during the growth due to inadequate conduction path for dc plasma current through S/D to contact clamps. Another problem was bubble formation due to dehydrogenation from the SiN_x and a-Si:H layer deposited using SiH_4 gas in PECVD. Thus, hydrogen is present in the films [10], [11]. During the 700-°C processing, dehydrogenation occurs and causes delamination bubbles. To mitigate the arcing problem, eight contact holes were patterned around the edge region of the wafer and etched through all the layers down to silicon wafer prior to the S/D deposition. Second, a preannealing procedure (600 °C, 1 h) was implemented to remove the hydrogen prior to the deposition of S/D Cr layer.

One of the main obstacles in integrating the VACNFs with TFTs was appropriate control of thin-film residual stress and subsequent thermal stress induced during the high-temperature process. In particular, the Cr S/D electrodes failed due to film delamination during the VACNF growth. It is well known that film delamination is related to the internal tensile stress [12]. Gleskova *et al.* [13] have reported on TFT failure due to mechanical strain induced by high processing temperature. Following the work of Misra *et al.* [14], we measured the stress of Cr films as a function of substrate bias. Without substrate bias during sputtering, Cr has a tensile stress of 1–2 GPa; however, when sputtered with 5-W substrate power, the stress was reduced to below 10 MPa and, subsequently, survived the VACNF growth. Fig. 2(a) shows the cumulative stress of each layer in the TFT after optimization, showing that the cumulative stress is compressive.

To determine whether the silicon film crystallizes during the VACNF growth, Fig. 2(b) shows a Raman and X-ray diffraction spectra of the silicon layer after VACNF growth and wet etching the requisite chromium layer. It is clear that the silicon crystallized and that a chromium silicide ($CrSi_2$) forms during the 700-°C dc-PECVD process. Formation of $CrSi_2$ has been reported to facilitate the silicon crystallization process [15].

Fig. 3 compares the current–voltage transfer characteristics of (a) TFT device fabricated without VACNFs and (b) a completed TFT-VACNF device. The on/off current ratio, the OFF-state leakage current, and the subthreshold swing of TFT calculated from Fig. 3(a) were $\sim 10^5$, $\sim 3 \times 10^{-11}$ A at $V_{\rm ds} =$ 10.1 V, and 0.92 V/dec at $V_{\rm ds} = 0.1$ V, respectively. The TFT-VACNF results from Fig. 3(b) were $\sim 10^4$, $\sim 9 \times 10^{-10}$ A at $V_{\rm ds} = 10.1$ V, and 1.87 V/dec at $V_{\rm ds} = 0.1$ V, respectively. The field-effect mobilities for the TFT and TFT-VACNF devices were determined to be 0.49 and 0.27 $\rm cm^2/V \cdot s$, respectively, at $V_{\rm ds} = 0.1$ V using linear portion of the $I_{\rm ds}-V_g$ plot. Furthermore, the threshold voltage was $\sim$0 V for TFT and $\sim$2.5 V for TFT-VACNF. The degradation of the device characteristics is attributed to the silicon and silicon nitride dehydrogenation, silicon crystallization, and silicide formation, as briefly discussed below.

The observed increase in the threshold voltage for the VACNF devices is attributed to the dehydrogenated silicon and

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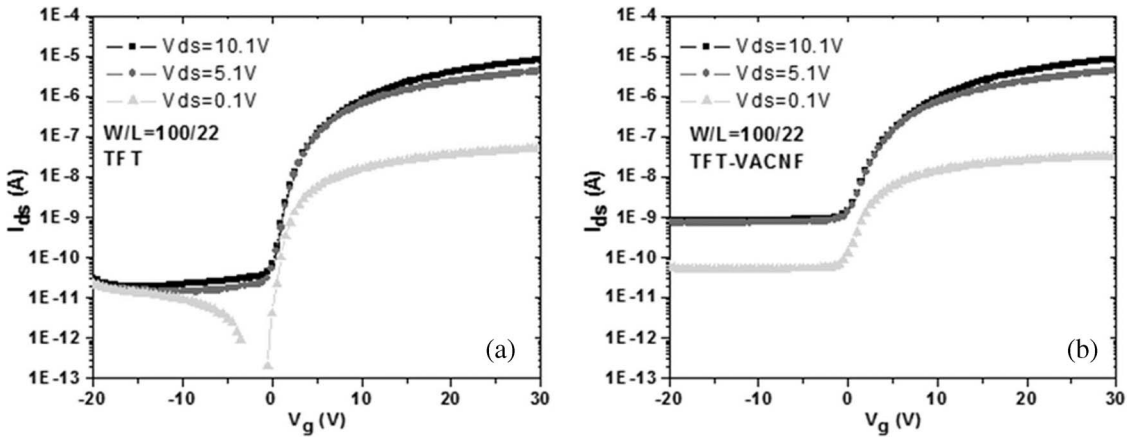


Fig. 3. Current–voltage transfer characteristics of the devices. (a) TFT fabricated without VACNF integration process. (b) TFT-VACNF devices.

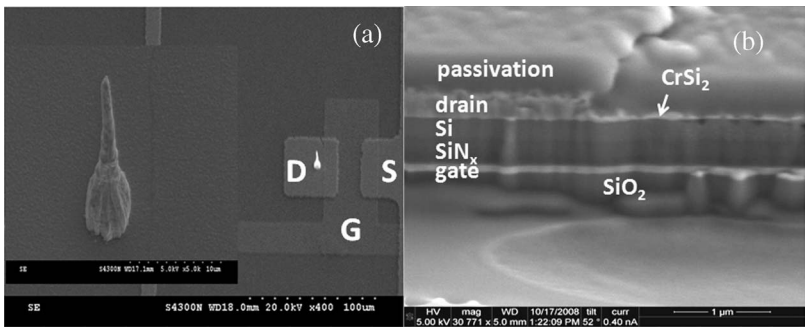


Fig. 4. Scanning electron micrographs of an individual element of TFT array with VACNFs integrated onto the devices. (a) Fabricated TFT-VACNF device; inset shows high-resolution images of VACNF, which is half-covered with passivation SiN_x film (images were tilted 30°), and (b) a focus ion beam milled cross-sectional image of the channel region.

silicon nitride, which leads the increase of defect density in the bulk and at the interface [16], [17]. It is surprising that the TFT-VACNF device has lower mobility and higher subthreshold swing because the silicon was crystallized during the VACNF growth process. We surmise that the lower mobility is due to $CrSi_2$ segregated into the polysilicon grain boundaries, which act as scattering centers for electrons. High-resolution scanning electron microscope (SEM) imaging (not shown) revealed some high-brightness "spikes" in the channel region which we believe to be evidence of the $CrSi_2$ segregation. The higher OFF-state current for the TFT-VACNF device is also ascribed to segregated $CrSi_2$ as well as unpassivated grain boundaries due to dehydrogenation [18]. The fact that the reverse bias leakage is relatively constant, instead of gradually increasing, is different than typical polysilicon TFTs and is not fully understood at this time. Fig. 4 shows SEM images illustrating (a) VACNFs successfully integrated onto the TFT array and (b) demonstrates a cross-sectional view of the channel region. The specific layers in the TFT device and evidence of the resultant $CrSi_2$ layer are labeled.

IV. Conclusion

In summary, a TFT array with integrated VACNF grown by Ni catalyst in dc-PECVD has been fabricated and characterized. To accommodate the dc-PECVD process, a contact via was etched to ground the prepatterned S/D electrode to the silicon substrate. To reduce bubbles and film delamination from the hydrogen entrapped from SiH_4 PECVD processing, a dehydrogenation preanneal was performed prior to S/D metal deposit. Moreover, to minimize the residual stress in the S/D layer and prevent delamination during VACNF growth, the internal stress of Cr film was controlled by applying a suitable (5 W) substrate bias during sputtering. Although the device performance was degraded by VACNF growth process, this device provides great potential to perform electroanalytical function with a high spatial density of electrodes engineered to probe live cells or other biological materials.

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